PCT

WORLD INTELLECTUAL PROPERTY ORGANIZATION
International Bureau

INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification 5 : H01L 23/48, 25/00

A1

(11) International Publication Number: WO 94/01887

(43) International Publication Date: 20 January 1994 (20.01.94)

(21) International Application Number: PCT/US93/06315

(22) International Filing Date: 2 July 1993 (02.07.93)

(30) Priority data:
07/909,597 7 July 1992 (07.07.92) US

(71) Applicant *(for all designated States except US)*: RTB TECHNOLOGY, INC. [US/US]; 3500 West Balcones Center Drive, Austin, TX 78759 (US).

(72) Inventors. and
(75) Inventors/Applicants *(for US only)*: GARTH, Emory, C. [US/US]; 1111 West 12th Street, Suite 108, Austin, TX 78703 (US). LANKFORD, Clive, III [US/US]; 13635 Rutledge Spur, Austin, TX 78729 (US).

(74) Agents: SIGMOND, David, M. et al.; 3500 West Balcones Center Drive, Austin, TX 78759 (US).

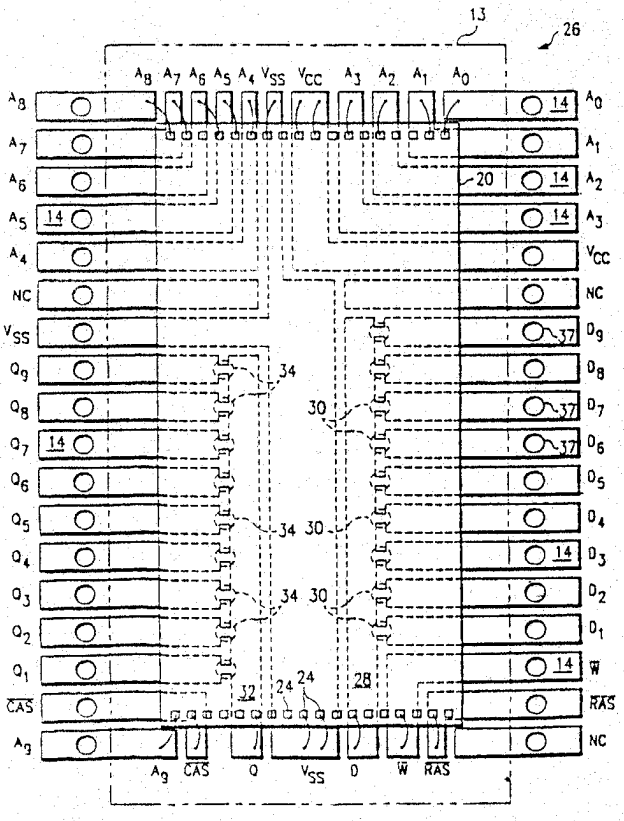
(81) Designated States: AT, AU, BB, BG, BR, CA, CH, CZ, DE, DK, ES, FI, GB, HU, JP, KP, KR, LK, LU, MG, MN, MW, NL, NO, NZ, PL, PT, RO, RU, SD, SE, SK, UA, US, VN, European patent (AT, BE, CH, DE, DK, ES, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, ML, MR, NE, SN, TD, TG).

Published
With international search report.

(54) Title: HIGH DENSITY MEMORY AND METHOD OF FORMING THE SAME

(57) Abstract

A high density memory module (10) includes a plurality of subassemblies (12), each subassembly (12) including a memory circuit (20), a lead frame (26) having a plurality of leads (14) coupled to the memory circuit (20) and encapsulating material (13) surrounding the memory circuit (20) and lead frame (26) such that the leads (14) extend outwardly from the encapsulating material (13). The memory module (10) is easily assembled and provides high density storage capability with convective heat transfer to reduce the temperature within the stack of subassemblies (12). A single lead frame (26) may be selectively addressed for use with each subassembly (12) within the memory module (10).



FOR THE PURPOSES OF INFORMATION ONLY

Codes used to identify States party to the PCT on the front pages of pamphlets publishing international applications under the PCT.

AT	Austria	**FR**	France	**MR**	Mauritania
AU	Australia	**GA**	Gabon	**MW**	Malawi
BB	Barbados	**GB**	United Kingdom	**NE**	Niger
BE	Belgium	**GN**	Guinea	**NL**	Netherlands
BF	Burkina Faso	**GR**	Greece	**NO**	Norway
BG	Bulgaria	**HU**	Hungary	**NZ**	New Zealand
BJ	Benin	**IE**	Ireland	**PL**	Poland
BR	Brazil	**IT**	Italy	**PT**	Portugal
BY	Belarus	**JP**	Japan	**RO**	Romania
CA	Canada	**KP**	Democratic People's Republic of Korea	**RU**	Russian Federation
CF	Central African Republic			**SD**	Sudan
CG	Congo	**KR**	Republic of Korea	**SE**	Sweden
CH	Switzerland	**KZ**	Kazakhstan	**SI**	Slovenia
CI	Côte d'Ivoire	**LI**	Liechtenstein	**SK**	Slovak Republic
CM	Cameroon	**LK**	Sri Lanka	**SN**	Senegal
CN	China	**LU**	Luxembourg	**TD**	Chad
CS	Czechoslovakia	**LV**	Latvia	**TG**	Togo
CZ	Czech Republic	**MC**	Monaco	**UA**	Ukraine
DE	Germany	**MG**	Madagascar	**US**	United States of America
DK	Denmark	**ML**	Mali	**UZ**	Uzbekistan
ES	Spain	**MN**	Mongolia	**VN**	Viet Nam
FI	Finland				

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US93/06315

A. CLASSIFICATION OF SUBJECT MATTER

IPC(5) :H01L 23/48, 25/00
US CL :257/684, 723
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 257/684, 723, 724, 725

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

APS, search terms: memory module, subassembly, lead frame

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
x	US, A, 5,028,986 (Sugano et al.) 02 July 1991, col. 5, line 35 through col. 18, line 64.	1-12

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

*	Special categories of cited documents:	"T"	later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"A"	document defining the general state of the art which is not considered to be part of particular relevance	"X"	document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"E"	earlier document published on or after the international filing date	"Y"	document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"L"	document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	"&"	document member of the same patent family
"O"	document referring to an oral disclosure, use, exhibition or other means		
"P"	document published prior to the international filing date but later than the priority date claimed		

Date of the actual completion of the international search	Date of mailing of the international search report
02 SEPTEMBER 1993	09 SEP 1993

Name and mailing address of the ISA/US	Authorized officer
Commissioner of Patents and Trademarks Box PCT Washington, D.C. 20231	DAVID B. HARDY
Facsimile No. NOT APPLICABLE	Telephone No. (703) 308-4092

DESCRIPTION

HIGH DENSITY MEMORY AND METHOD OF FORMING THE SAME

Technical Field

This invention relates in general to integrated circuits, and more particularly to a high density memory module.

Background Art

High speed digital processing systems often require large amounts of high speed memory. While mass memory devices, such as hard disks, are capable of storing large amounts of information, the speed associated with these devices is insufficient for many purposes. In many applications, speed considerations are satisfied by storing large amounts of information in semiconductor memory, such as dynamic random access memory (DRAM) and static random access memory (SRAM).

Normally, semiconductor memory is packaged in DIPs (dual-inline packages), ZIPs (Zip-Zag Inline Packages), SOJs (Small Outline J-leaded), SIPs (single-inline packages), and SIMMs (single-inline memory module). In these packaging options, the package itself is many times the size of the semiconductor integrated circuit which performs the memory function. Applications which need a large amount of memory or provide user-upgradeable sockets for increasing the size of the memory often dedicate a large area on the circuit board for the memory chips.

Currently, one megabit DRAMs are the industry standard memory circuits, with four megabit memory circuits now reaching price parity with the one megabit circuits. While board space is reduced by the improved chip densities, the need for increased memory generally outpaces the speed with which memory circuit densities are increased.

A prior art interim solution to chip densities has been "piggy-backing" DIPs such that a stack of memory circuits are interconnected to emulate a higher density memory circuit. Piggy-backing has resulted in several problems and is seldom used anymore.

A more modern solution is to interconnect a stack of memory circuits which are not contained in their typical package thereby effecting a greater density. An example of this approach is "3-D Memory Multichip Modules" from Texas Instruments. Present implementations of this approach present significant problems. First, the stacked memory circuits suffer from thermal problems, particularly affecting those memory circuits in the middle of the stack where the heat is not adequately dissipated. Second, the complexity of manufacturing the stacked memory circuits results in a relatively high cost in comparison with other packaging options. Third, testing of the memory circuits is difficult.

Disclosure of Invention

According to the present invention, a high density memory module and method of forming the same is provided. The memory module has safe

thermal characteristics, high testability, and may be fabricated using uncomplicated procedures.

The memory module comprises a plurality of memory subassemblies, wherein each subassembly includes a memory circuit, a lead frame having a plurality of leads coupled to the memory circuit, and encapsulating material surrounding the memory circuit and the lead frame, such that the leads extend outwardly from the encapsulating material to allow convective heat transfer. Connectors couple the respective leads of the memory subassemblies outside the encapsulating material to electrically couple the memory circuits.

Advantageously, the leads extend outwardly from the encapsulating material such that each of the memory circuits may dissipate heat by conductive heat transfer through the leads to a convective surface. The convective surface area can be adjusted for optimum heat transfer by adjusting the length of the lead outside the encapsulating material. Further, packaging of the memory circuit by the encapsulating material may be performed such that the leads may be used for testing prior to final assembly.

In preferred embodiments, each lead frame has an identical layout such that predefined portions of the lead frame may be removed to provide a unique circuit configuration corresponding to the position of the memory circuit in the stack. The use of a single lead frame layout greatly simplifies the construction of the memory module.

Brief Description of Drawings

Reference is now made to the following descriptions taken in conjunction with the accompanying drawings, in which:

FIGURE 1a illustrates a perspective view of the high density memory module (HDMM);

FIGURE 1b illustrates a pin-out for the HDMM of FIGURE 1a;

FIGURE 2 illustrates a schematic representation of the high density memory module;

FIGURE 3a illustrates a top view of a 1 M x 1 DRAM circuit showing the interconnection pads;

FIGURE 3b illustrates a top view of a lead frame;

FIGURE 4a illustrates a top view of the encapsulated RAM prior to assembly, showing the lead frame test points;

FIGURE 4b illustrates an encapsulated DRAM subassembly prior to final assembly with cutaway views of the memory circuit and lead frame;

FIGURE 5 illustrates a bottom perspective view of the bottom header of the memory module;

FIGURE 6 illustrates an exploded view of the memory module;

FIGURE 7a illustrates a top view of a 1 M x 4 DRAM circuit showing the interconnection pads; and

FIGURE 7b illustrates a top view of a lead frame for a 1 M x 40-bit HDMM.

Best Mode for Carrying Out the Invention

In referring to FIGUREs 1-7 of the drawings, like numerals are used for like and corresponding parts of the various drawings.

FIGURE 1 illustrates a perspective view of a high density memory module (HDMM). The HDMM 10 comprises a plurality of stacked subassemblies 12 having protruding leads 14. Pins 16 are positioned through respective aligned leads 14. The pins 16 terminate in ends 18 which may be attached directly to a circuit board or inserted into a socket which is attached to a circuit board. A bottom header 19a and top header 19b are positioned at the bottom and top, respectively, of the HDMM 10.

Each subassembly 12 includes a memory circuit coupled to a lead frame which has been encapsulated in a dielectric packaging material 13, with the leads 14 protruding from the packaging material. The lead frames are described in greater detail in connection with FIGURE 3b. Pins 16 provide electrical connections in the third (vertical) dimension to distribute the appropriate signals to multiple memory circuits. The subassemblies 12 may be configured in groups of eight (or nine to include a

parity bit) to form bytes of digital data. The number of stacked subassemblies may be increased or decreased in order to provide a desired word size or an alternative configuration. For purposes of illustration, the HDMM will be described in connection with a 1 Mbit x 9 dynamic random access memory module, although other configurations can be easily designed.

In addition to distributing signals from the memory circuits, the lead frames also provide thermal management. Heat from the memory circuits is conducted to the exterior of the HDMM by leads 14, which are cooled by the ambient air.

Using a memory circuit having dimensions of approximately 0.180 x 0.400 inches (.4572 x 1.016 cm), an HDMM 10 may be formed having dimensions of approximately 0.340 x 0.475 x 0.435 inches (.8636 x 1.2065 x 1.1049 cm) using a stack of nine subassemblies 12. The HDMM achieves a packaging density approaching the practical maximum possible as limited by the physical size of the silicon, the lead frame and the necessary encapsulation for environmental protection. Current one megabit memory circuits have dimensions of approximately .243 x .115 inches (.6172 x .2921 cm), which significantly reduces the size of the silicon and improvements in encapsulation techniques would reduce the size of the HDMM.

FIGURE 1b illustrates a pin-out of the HDMM 10. For the illustrated embodiment of a 1 Mbit x 9 DRAM module ten address pins (A_0-A_9), nine data inputs (D_1-D_9), and nine data outputs (Q_1-Q_9) are provided. $\overline{CAS}$, $\overline{RAS}$ and $\overline{W}$ provide the control signals to read and write to the HDMM. V_{ss} and V_{cc} provide the power to the HDMM.

FIGURE 2 illustrates a schematic representation of the interconnections between the memory circuits and the pins of the HDMM 10. The pin numbers, referenced to the pin-out of FIGURE 1b, are shown parenthetically. Nine one-megabit memory circuits 20, referred to individually as memory circuits 20a-20i, are used to form the HDMM 10. Address pins A_0-A_9 are coupled to respective inputs for each of the memory circuits 20a-20i. Similarly, V_{cc}, V_{ss}, $\overline{RAS}$, $\overline{CAS}$ and $\overline{W}$ pins are coupled to

respective inputs of the memory circuits 20a-20i. The data inputs D_1-D_9 and data outputs Q_1-Q_9 are coupled to the data inputs (D) and data outputs (Q) of respective memory chips 20a-20i. Hence, D_1 is coupled to data input D of memory circuit 20a, D_2 is coupled to data input D of memory circuit 20b, $D_3$is coupled to data input D of memory circuit 20c, and so on. Similarly, Q_1 is coupled to data output Q of memory circuit 20a, $Q_2$is coupled to data output Q of memory circuit 20b, and Q_3 is coupled to data output Q of memory circuit 20c. Thus, for any given address, nine bits of data may be either written to, or read from, the HDMM 10. Decoupling capacitors 22a-d are coupled between V_{cc} and V_{ss}.

FIGURE 3a illustrates a top view of an exemplary memory circuit 20. Signals from the memory circuit 20, as shown in connection with the schematic of FIGURE 2, are available at pads 24. Connection between the pads 24 and the lead frame 26 (see FIGURE 3b) may be performed by wire bonding.

FIGURE 3b illustrates a lead frame 26 which is wire bonded to the memory circuit 20 shown in FIGURE 3a. The outline of the encapsulation packaging 13 and memory circuit 20 are shown for reference. In FIGURE 3b, the lead frame 26 is shown with the test points removed; the full lead frame prior to trimming is shown in greater detail in connection with FIGURE 4a. Each subassembly 12 comprises a lead frame 26 having its leads 14 wire bonded to the pads 24 of the memory circuit 20. The lead frame 26 is attached to the memory circuit 20 using a very thin adhesive, typically an epoxy, that provides mechanical support of the lead frame 26 during wire bonding and also provides a low thermal impedance path for heat flow from the semiconductor to the lead frame 26 which, in turn, conducts heat out of the HDMM 10 through a low thermal impedance path to convective surfaces for transfer into the ambient air. Typically, the lead frame 26 uses a copper alloy material; however, most lead frame materials will also be good heat conductors.

Importantly, a single lead frame configuration may be used in connection with any one of the subassemblies in the HDMM, regardless of

its position in the stack, thereby reducing the complexity of manufacture. The data input D of the memory circuit is coupled to a signal pad 28 which is electrically coupled via removable connections 30 to each of the leads 14 associated with pins D_1-D_9. To configure the lead frame 26 for a particular subassembly level, all but one of the removable connections 30 are removed. For example, the lead frame 26 coupled to memory circuit 20a will have the removable connections 30 associated with leads D_2-D_9 removed. Similarly, the lead frame 26 includes a signal pad 32 coupled to the data output Q of the memory circuit 20. The signal pad 32 is coupled to the leads 14 associated with data outputs Q_1-Q_9 via removable connections 34. Again, for a particular subassembly level, the removable connections 34 for all but one of the leads 14 associated with Q_1-Q_9 are removed. Thus, for memory circuit 20a, all removable connections 34 are removed except for the connector associated with the Q_1 lead. Hence, memory circuit 20a has its data input pad D coupled to the D_1 lead and has its data output pad Q coupled to the Q_1 lead. The subassemblies 12 are marked either during or after encapsulation to identify the unique data input/output configuration.

In the preferred embodiment, the leads 14 are spaced on 0.025 inch (0.0635 cm) centers outside of the encapsulating package and configured as shown with holes 37 located to provide a three-dimensional interconnect via pins 16.

Each subassembly 12 should undergo a complete electrical test and subsequent burn-in after encapsulation. FIGURE 4a illustrates the encapsulated memory circuit, showing the extended lead frame test points. Prior to encapsulation, the lead frame 26 has extended leads 36 with test points 38. The encapsulation process forms the subassemblies 12 with leads 14 still connected to extended leads 36. The extended leads are encapsulated in the secondary package 40 with the test points 38 exposed. Hence, at this point in the fabrication process, the memory circuits may be easily tested.

As shown in FIGURE 4b, the subassemblies 12 are separated from the secondary package 40 prior to assembly of the HDMM 10. FIGURE 4b illustrates a cutaway view showing the memory circuit 20 and lead frame 26 encapsulated within the package 13.

FIGURE 5 illustrates a bottom view of the bottom header 19a. The bottom header includes the four capacitors 22a-d (shown in FIGURE 2) coupled between the pins associated with V_{cc} and V_{ss}.

FIGURE 6 illustrates an exploded view of the HDMM 10 to show the assembly of the various parts. The subassemblies 12 are stacked, with each subassembly uniquely addressed using removable connections 30 and 34 such that each subassembly has a unique data input/output pin-out. The bottom header is placed at the bottom of the stack of subassemblies, with the capacitors 22a-d disposed away from the subassemblies, (*i.e.*, towards the circuit board) and the top header 19b is disposed above the stack of subassemblies 12. The pins 16 are disposed through the vertically aligned leads 14 and the holes in the headers 19a-b. A thin adhesive is used between each subassembly 12. Subsequent to placing the pins through the leads, the adhesive is cured and a reflow solder process is used on electrical joints using a high temperature solder to complete the assembly.

In the preferred embodiment, the bottom header 19a is fabricated from sheets of copper-clad high-temperature plastic that are subsequently drilled and etched or molded from high-temperature plastic and selectively copper-plated to provide the decoupling capacitor mounting pads and annular rings at each of the thirty-six holes. The top header 19b is fabricated similarly, but without the capacitor mounting pads.

Each of the individual components (headers 19a-b, unique subassemblies 12, and capacitors 22) may be packaged in embossed tape on reels to enhance material handling accuracy and to ease presentation to the assembly equipment. In the preferred embodiment, the assembly process successively places the components onto the thirty-six individual pins that are cut from individual rolls of round wire. The HDMM 10 may

be assembled in an inverted position such that the coined ends of the pins may more easily align with the hole pattern of each subassembly 12 in the stack.

After cleaning, each HDMM 10 may be electrically tested and placed in a temperature-cycle burn-in oven for final conditioning.

FIGUREs 7a-b illustrate a pin-out for a 1 M x 4-bit memory circuit and a lead frame configuration for implementing a 1 M x 40 bit memory, respectively. The 1 M x 4-bit memory circuit 42 comprises ten address lines (A_0-A_9), four data input/output signals (DQ_1-DQ_4), power signals (V_{cc}, V_{ss}) and control signals ($\overline{CAS}$, $\overline{RAS}$, $\overline{OE}$ and $\overline{W}$).

Each of the data input/output signals of the memory circuit 42 is coupled to an associated signal pad on the 1 megabit x 40 lead frame 44. Hence, input/output DQ_1 of memory circuit 42 is coupled to signal pad 46, input/output DQ_2 is coupled to signal pad 48, input/output DQ_3 is coupled to signal pad 50 and input/output DQ_4 is coupled to signal pad 52. Each of the signal pads 46-52 are coupled to a respective set of ten leads 14. Signal pad 46 is coupled to ten leads 14, labeled $DQ_1(1)$-$DQ_1(10)$, via removable connections 34 as described in connection with FIGURE 3b. Similarly, signal pad 48 is coupled to leads 14 labeled $DQ_2(1)$-$DQ_2(10)$, signal pad 50 is coupled to leads 14 labeled $DQ_3(1)$-$DQ_3(10)$ and signal pad 52 is coupled to leads 14 labeled $DQ_4(1)$-$DQ_4(10)$. The remaining connections between memory circuit 42 and lead frame 44 are the same as described in connection with FIGURE 3b.

For each subassembly level of the 1 M x 40 HDMM, the associated lead frame 44 will be uniquely identified by removing all but one of the removable connections 34 for each set of leads DQ_1-DQ_4. For example, at the first level, leads $DQ_1(1)$, $DQ_2(1)$, $DQ_3(1)$ and $DQ_4(1)$ will each be coupled to their respective signal pads while the remaining leads will be decoupled by removing removable connections 34. For a 1 M x 40 HDMM, ten levels of subassemblies will be needed.

While the previous embodiments described a 1 Mbyte DRAM module, other configurations could be similarly designed. For example, for a 1 M x

16 bit HDMM, the lead frame 26 could provide sixteen data input leads and sixteen data output leads (or eighteen input/output leads using byte parity) using 1 M x 1-bit memory circuits. Further, the address range of the HDMM could be increased by using a higher density memory circuit (for example, a 4 Mbit x 1 memory circuit) and providing additional address leads or by using additional subassembly chip select signals. Further, the HDMM could be used with other memory technologies such as static RAM and flash memory circuits.

Various changes, substitutions and alterations can be made herein without departing from the scope of the invention as defined by the appended claims.

CLAIMS

1. A memory module (10) comprising a plurality of memory subassemblies (12), each subassembly (12) comprising (i) a memory circuit (20), (ii) a lead frame (26) having a plurality of thermally and electrically conductive leads (14) with selected leads (14) electrically coupled to said memory circuit (20) and non-selected leads (14) electrically isolated from said memory circuit (20), and (iii) an encapsulating material (13) surrounding said memory circuit (20) and a portion of lead frame (26) wherein said leads (14) extend outwardly from said encapsulating material (13), said memory module (10) further comprising electrical connectors (16) coupled to portions of said leads (14) outside of said encapsulating material (13), characterized in that:

each of said leads (14) provides conductive heat transfer from said memory circuit (20) to an area outside said encapsulating material (13) and convective heat transfer from the portions of said leads (14) extending outside of said encapsulating material (13); and

at least one of said selected leads (14) is selectably coupled to said memory circuit (20).

2. A memory module (10) comprising a lead frame (26), a memory circuit (20) and an encapsulating material (13), said lead frame (26) comprising (i) a plurality of first leads (14) electrically coupled to said memory circuit (20) and extending outside said encapsulating material (13), (ii) a plurality of second leads (14) extending outside said encapsulating material (13), and (iii) a plurality of conductive surfaces (28,32) electrically coupled to said memory circuit (20) and completely surrounded by said encapsulating material (13), characterized by:

said lead frame (26) further comprising removable connectors (30,34) for selectively coupling said second leads (14) to said conductive surfaces (28,32).

3. A method of forming a memory module (10), comprising the steps of (i) providing a plurality of lead frames (26) containing leads (14), (ii) electrically coupling a plurality of memory circuits (20) to respective lead frames (26), (iii) adhering said memory circuits (20) to said respective lead frames (26), (iv) encapsulating said coupled memory circuits (20) and portions of said respective lead frames (26) to form memory subassemblies (12) such that outer ends of leads (14) extend out from an encapsulating material (13), and (v) electrically coupling said subassemblies (12) by interconnecting said outer ends of leads (14), characterized by:

configuring a plurality of identical lead frames (26) in step (i) such that each of said plurality of lead frames (26) provides a unique input/output data path for the respective memory circuit (20).

4. A three-dimensional memory module (10) comprising (I) a plurality of horizontally-oriented, vertically-stacked memory subassemblies (12), each memory subassembly (12) comprising (i) a memory circuit (20) comprising a plurality of bonding pads (24) for receiving data input signals, address signals, control signals and power supply voltages, and for sending data output signals, (ii) a lead frame (26) formed of thermally and electrically conductive material comprising a plurality of outwardly extending leads (14) wherein selected leads (14) are electrically coupled to said pads (24) whereas non-selected leads (14) are electrically isolated from said pads (24), (iii) a mechanical coupling element between said memory circuit (20) and said lead frame (26), and (iv) a dielectric material (13) surrounding and encapsulating said memory circuit (20) and a portion of said lead frame (26) wherein the unencapsulated portion of said lead frame (26) includes outer portions of leads (14), said outer portions of leads (14) protruding from said dielectric material (13) and providing convective surface areas to ambient air outside said dielectric material (13), wherein said lead frames (26) are positioned so that said outer portions of leads (14) are aligned in vertical columns, and (II) a plurality of separate, spaced vertically-oriented electrical connectors (16) positioned outside said

dielectric material (13) wherein each electrical connector (16) electrically couples the outer portion of each lead (14) in a single vertical column of leads (14) without electrically coupling the outer portion of any leads (14) outside said single vertical column, characterized in that:

a thermal coupling element is between said memory circuit (20) and said lead frame (26);

said lead frame (26) provides a low thermal impedance path that allows said memory circuit (20) to dissipate heat by conductive heat transfer through said thermal coupling element into said lead frame (26) within said dielectric material (13) and through said lead frame (26) within said dielectric material (13) to the convective surface areas of said outer portions of leads (14);

said lead frames (26) are configured so that each data input pad (24) of each memory circuit (20) is the only data input pad (24) in the memory module (10) which is electrically coupled to a selected electrical connector (16), thereby providing each memory subassembly (12) with a unique data input configuration corresponding to the position of the memory subassembly (12) in the stack; and

said lead frames (26) are configured so that each data output pad (24) of each memory circuit (20) is the only data output pad in the memory module (10) which is electrically coupled to a selected electrical connector (16), thereby providing each memory subassembly (12) with a unique data output configuration corresponding to the position of the memory subassembly (12) in the stack.

5. The memory module (10) of claim 4 wherein:

said outer portions of leads (14) of each lead frame (26) have identical layouts, said dielectric materials (13) have identical layouts, and said memory subassemblies (12) are stacked adjacent to one another;

said electrical connectors (16) are formed of thermally and electrically conductive metal, provide convective surface areas to said ambient air, and are electrically and thermally coupled to said vertical columns of leads (14);

the entire surfaces of said outer portions of leads (14) and the entire surfaces of said electrical connectors (16) between the top and bottom of the stack are convective surface areas; and

said lead frame (26) is formed with opposing major surfaces parallel to one another, said memory circuit (20) is disposed over said leads (14), said mechanical coupling element mechanically couples said memory circuit (20) to portions of said leads (14) beneath said memory circuit (20), said thermal coupling element thermally couples said memory circuit (20) to portions of said leads (14) beneath said memory circuit (20); and metallic bonds electrically couple said pads (24) to said selected leads (14).

6. The memory module (10) of claim 4 wherein:

said memory circuit (20) is disposed over said leads (14);

said mechanical coupling element mechanically couples said memory circuit (20) to portions of said leads (14) beneath said memory circuit (20);

said thermal coupling element thermally couples said memory circuit (20) to portions of said leads (14) beneath said memory circuit (20); and

metallic bonds electrically couple said pads (24) to said selected leads (14).

7. The memory module (10) of claim 6 wherein:

said lead frame (26) consists of said leads (14);

said leads (14) have flat and parallel top and bottom surfaces within said dielectric material (13);

said memory circuit (20) is formed with a flat bottom surface facing said leads (14) and opposite said pads (24); and

said mechanical coupling element adhesively connects the bottom surface of said memory circuit (20) to the top surfaces of said leads (14) therebeneath.

8. The memory module (10) of claim 4 wherein all low thermal impedance paths between said memory circuit (20) and said ambient air must include said thermal coupling element and said lead frame (26).

9. The memory module (10) of claim 4 wherein:

said memory circuit (20) and said lead frame (26) are the only thermally conductive materials in contact with said thermal coupling element; and

said lead frame (26) is the only thermally conductive material both within and in contact with said dielectric material (13).

10. The memory module (10) of claim 4 wherein said mechanical and thermal coupling elements are a single adhesive material in full surface contact with one surface of said memory circuit (20).

11. The memory module (10) of claim 4 wherein:

all electrical interconnections between said pads (24) and circuitry outside said dielectric material (13) must include said selected leads (14);

in each of said memory subassemblies (12), excluding said power supply pads (24), each of said pads (24) is coupled to a single selected lead (14) and each of said selected leads is coupled to a single pad (24);

said memory subassemblies (12) have identical power supply, control signal and address signal configurations, and said electrical connectors (16) connect all power supply voltages, control signals and address signals in common among said memory circuits (20);

some but not all of said selected leads (14) in a given memory assembly (12) include a removable connection surrounded by said encapsulating material (13); and

each of said non-selected leads (14) in a given memory subassembly (12) is electrically coupled to a single electrical connector (16) which is electrically coupled to a single pad (24) on a single memory circuit (20) in another memory subassembly (12), said single pad (24) functioning as at least one of said data input pad (24) or said data output pad (24).

12. The memory module (10) of claim 4 wherein:

said unique data input and data output configurations for said memory circuit (20) are provided by several opened connections on the encapsulated portion of said lead frame (26);

each non-selected lead (14) is rendered electrically isolated from said pads (14) by a single opened connection;

said data input pad (24) is electrically coupled to a single selected lead (14) which includes a removable connection (30);

said data output pad (24) is electrically coupled to a single selected lead (14) which includes a removable connection (34); and

each of said lead frames (26) has a uniquely positioned removable connection (30,34) included in one but not all of said selected leads (14).

FIG. 1a

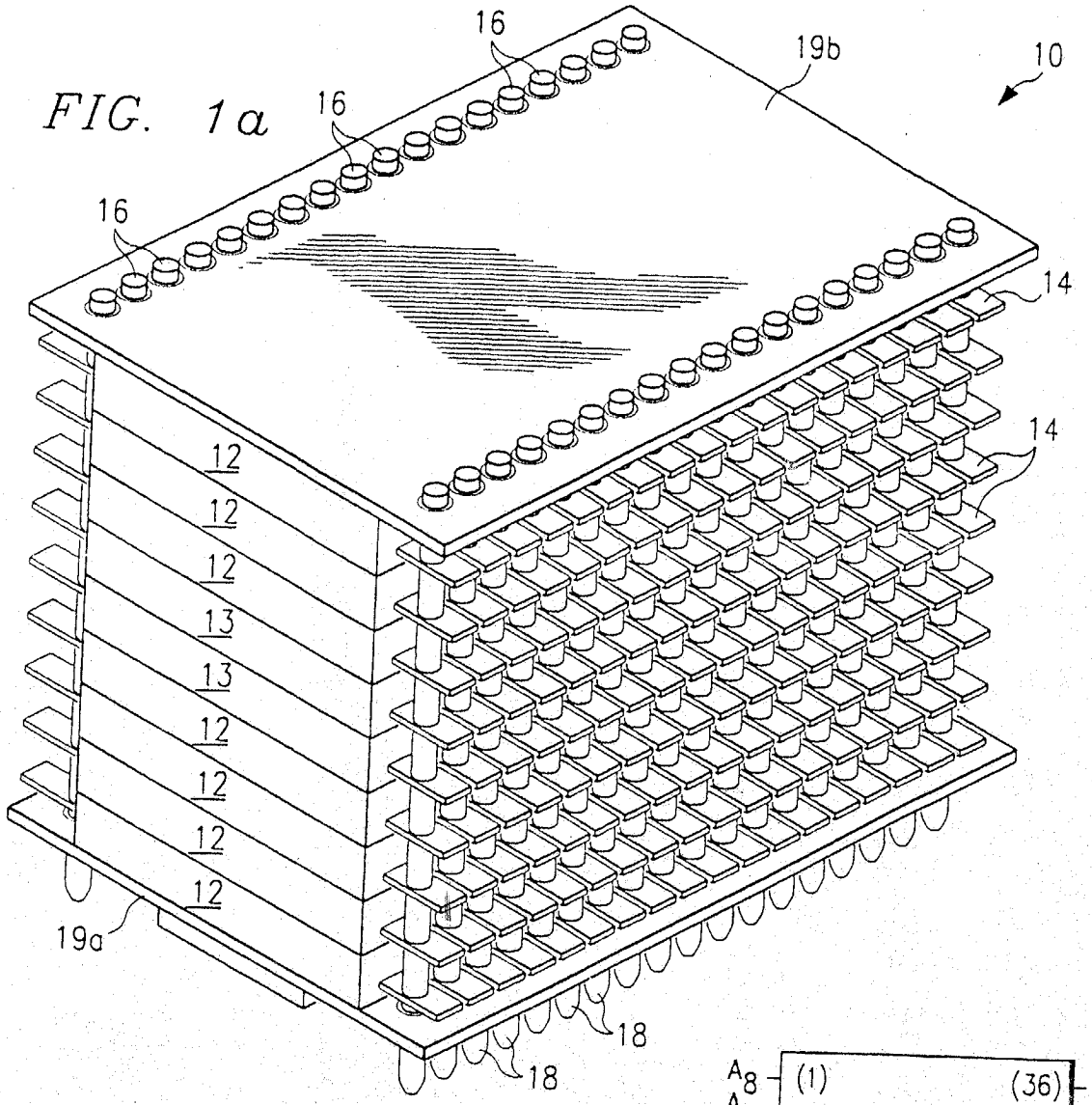

16
16
16
19b
10
14
14
12
12
12
13
13
12
12
12
12
19a
18
18

FIG. 1b

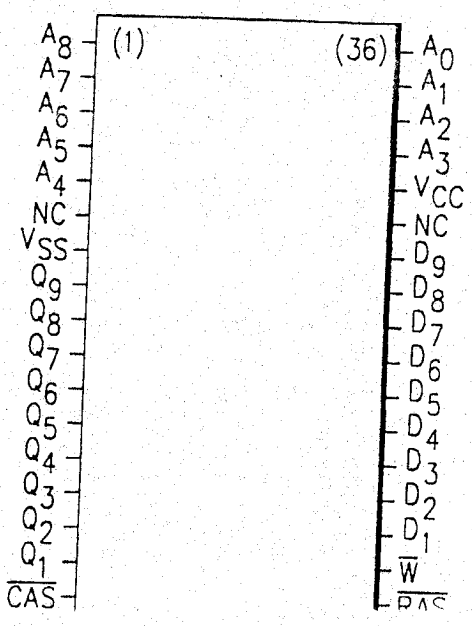
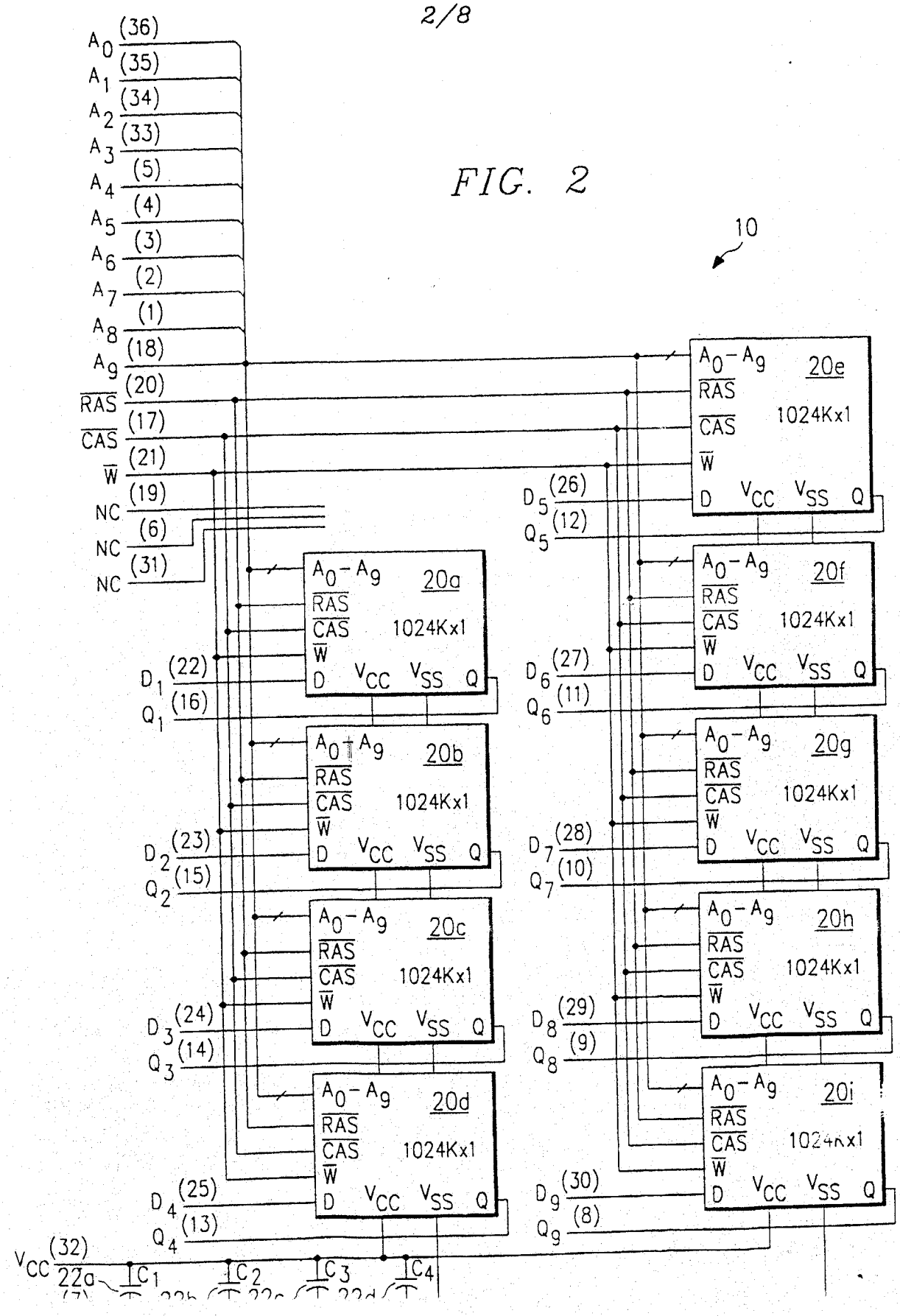

(1)
(36)
A8
A7
A6
A5
A4
NC
VSS
Q9
Q8
Q7
Q6
Q5
Q4
Q3
Q2
Q1
CAS
A0
A1
A2
A3
VCC
NC
D9
D8
D7
D6
D5
D4
D3
D2
D1
W

FIG. 2


10
A0 (36)
A1 (35)
A2 (34)
A3 (33)
A4 (5)
A5 (4)
A6 (3)
A7 (2)
A8 (1)
A9 (18)
RAS (20)
CAS (17)
W (21)
NC (19)
NC (6)
NC (31)
20a
20b
20c
20d
20e
20f
20g
20h
20i
A0 - A9
RAS
CAS
W
D
Q
VCC
VSS
1024Kx1
D1 (22)
Q1 (16)
D2 (23)
Q2 (15)
D3 (24)
Q3 (14)
D4 (25)
Q4 (13)
D5 (26)
Q5 (12)
D6 (27)
Q6 (11)
D7 (28)
Q7 (10)
D8 (29)
Q8 (9)
D9 (30)
Q9 (8)
VCC (32)
22a
C1
C2
C3
C4

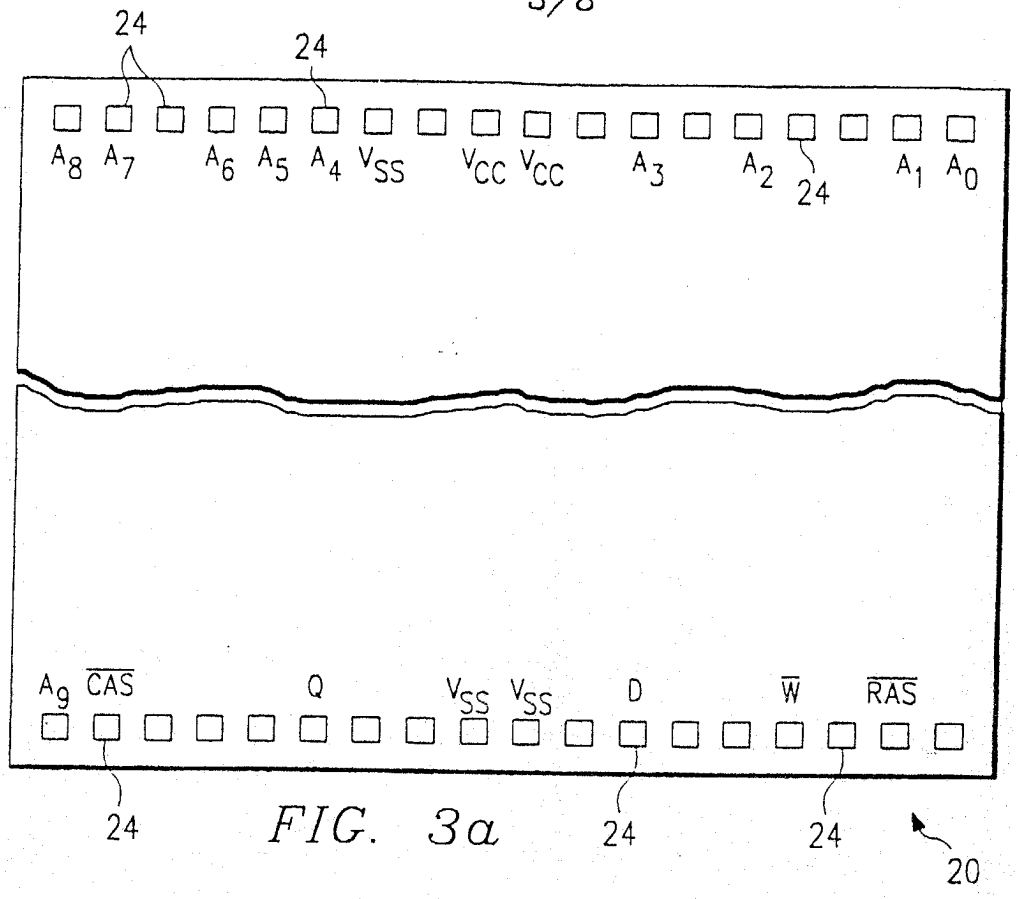

24
24
A8 A7 A6 A5 A4 VSS VCC VCC A3 A2 24 A1 A0
A9 CAS Q VSS VSS D W RAS
24
24
24
20

FIG. 3a

FIG. 5

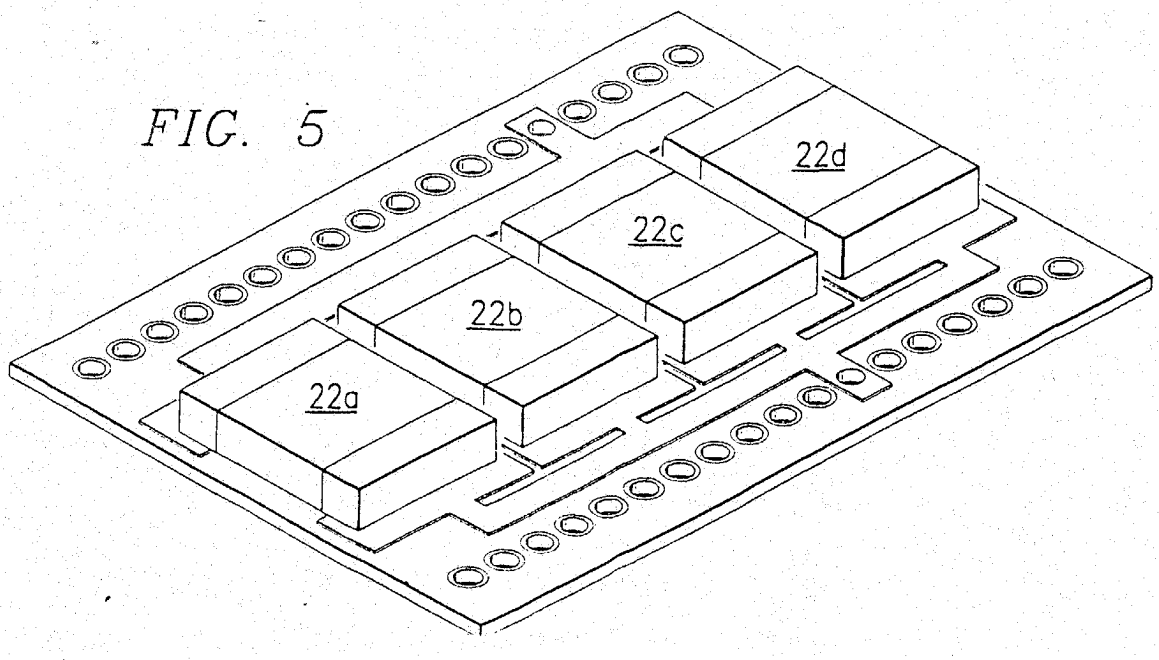
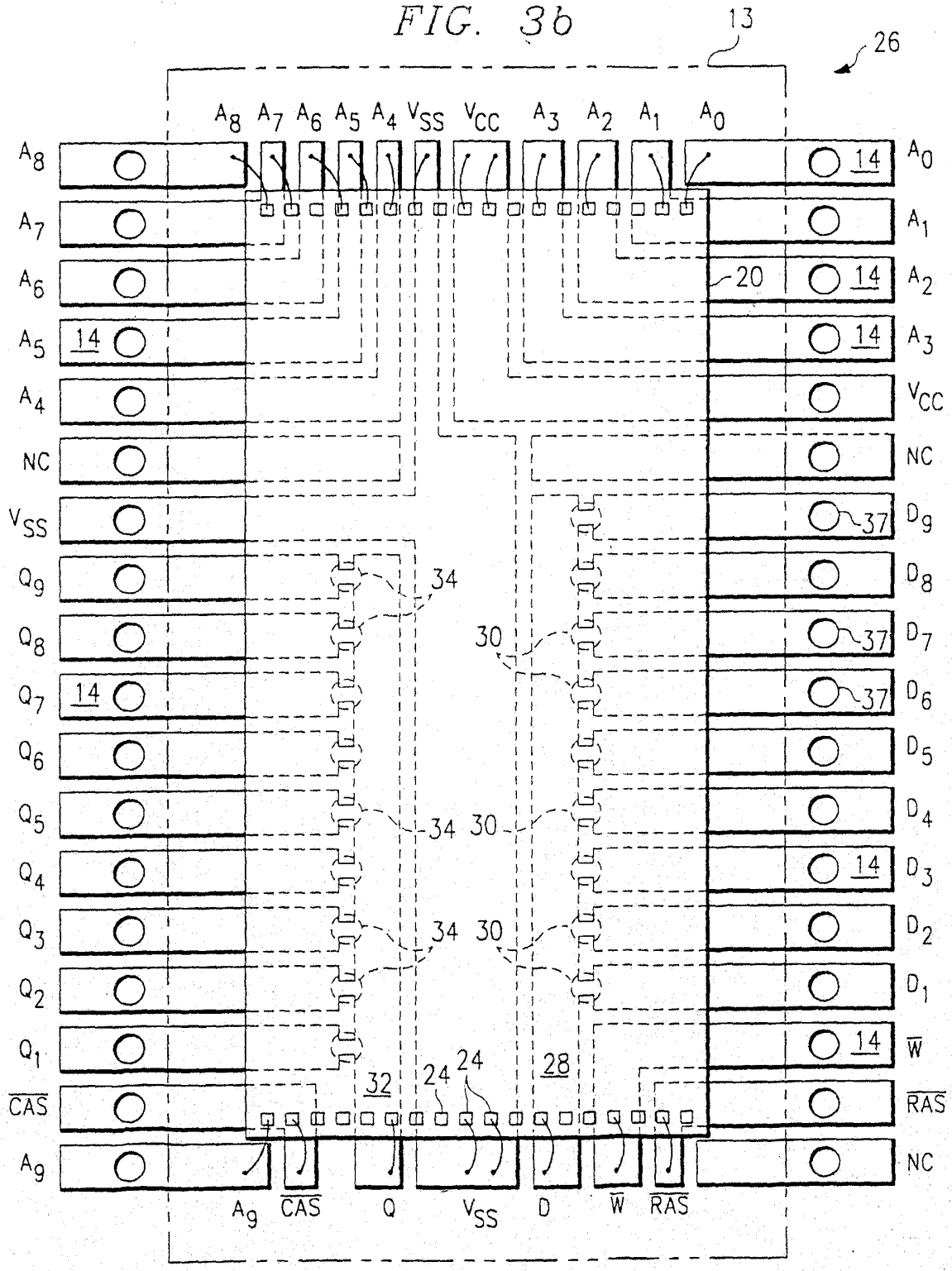

22d
22c
22b
22a

FIG. 3b


13
26
A8 A7 A6 A5 A4 VSS VCC A3 A2 A1 A0
A8
A7
A6
A5
A4
NC
VSS
Q9
Q8
Q7
Q6
Q5
Q4
Q3
Q2
Q1
CAS
A9
A0
A1
A2
A3
VCC
NC
D9
D8
D7
D6
D5
D4
D3
D2
D1
W
RAS
NC
14
20
34
30
32
24
28
A9 CAS Q VSS D W RAS

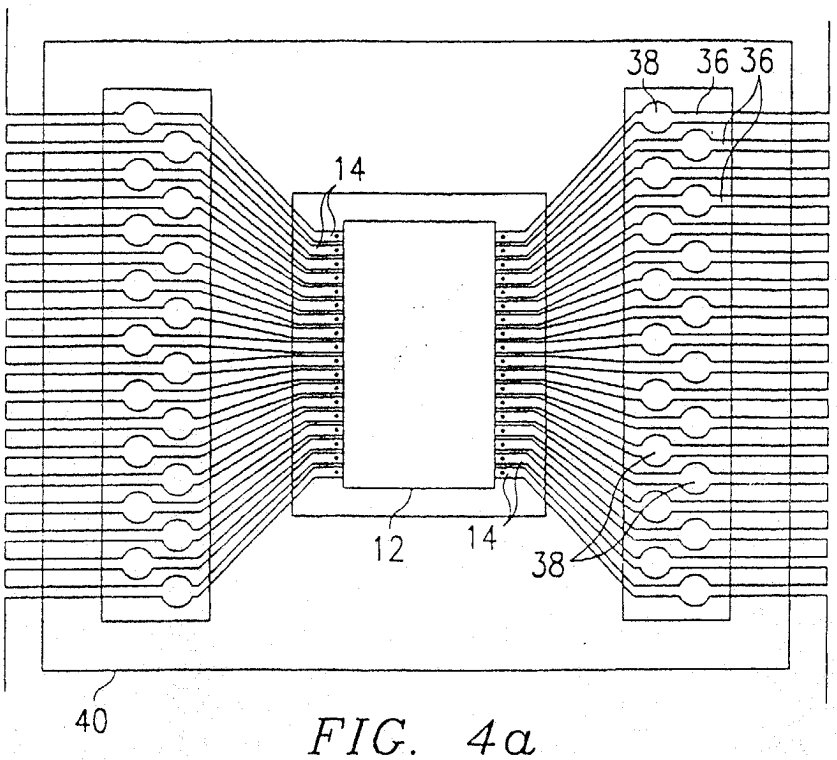


FIG. 4a

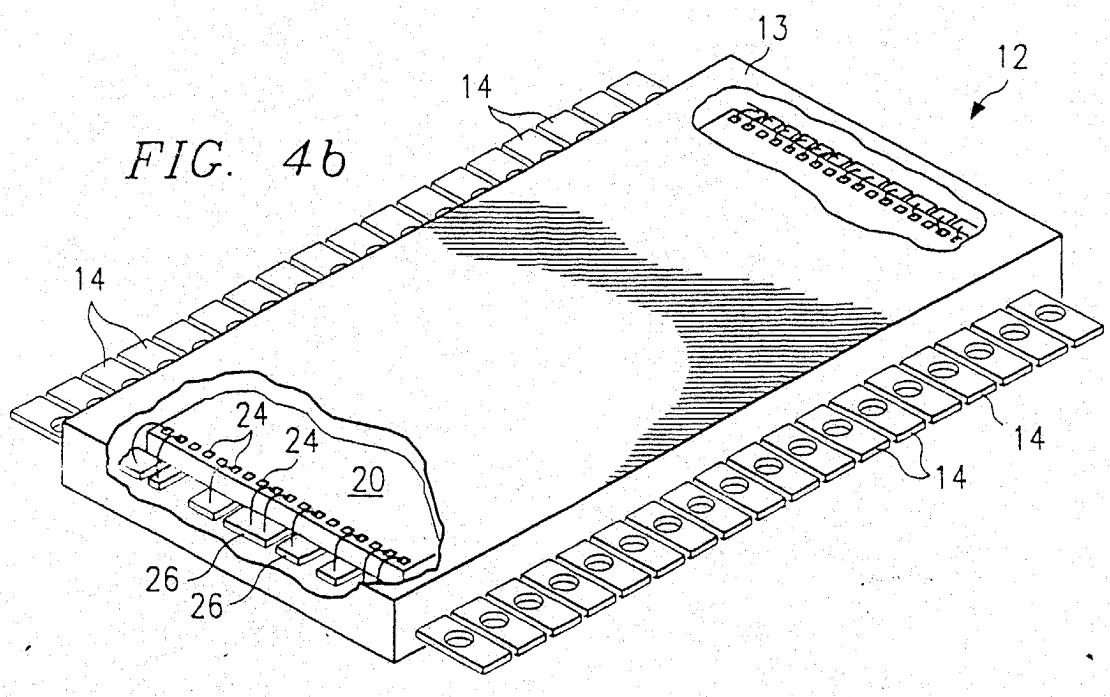
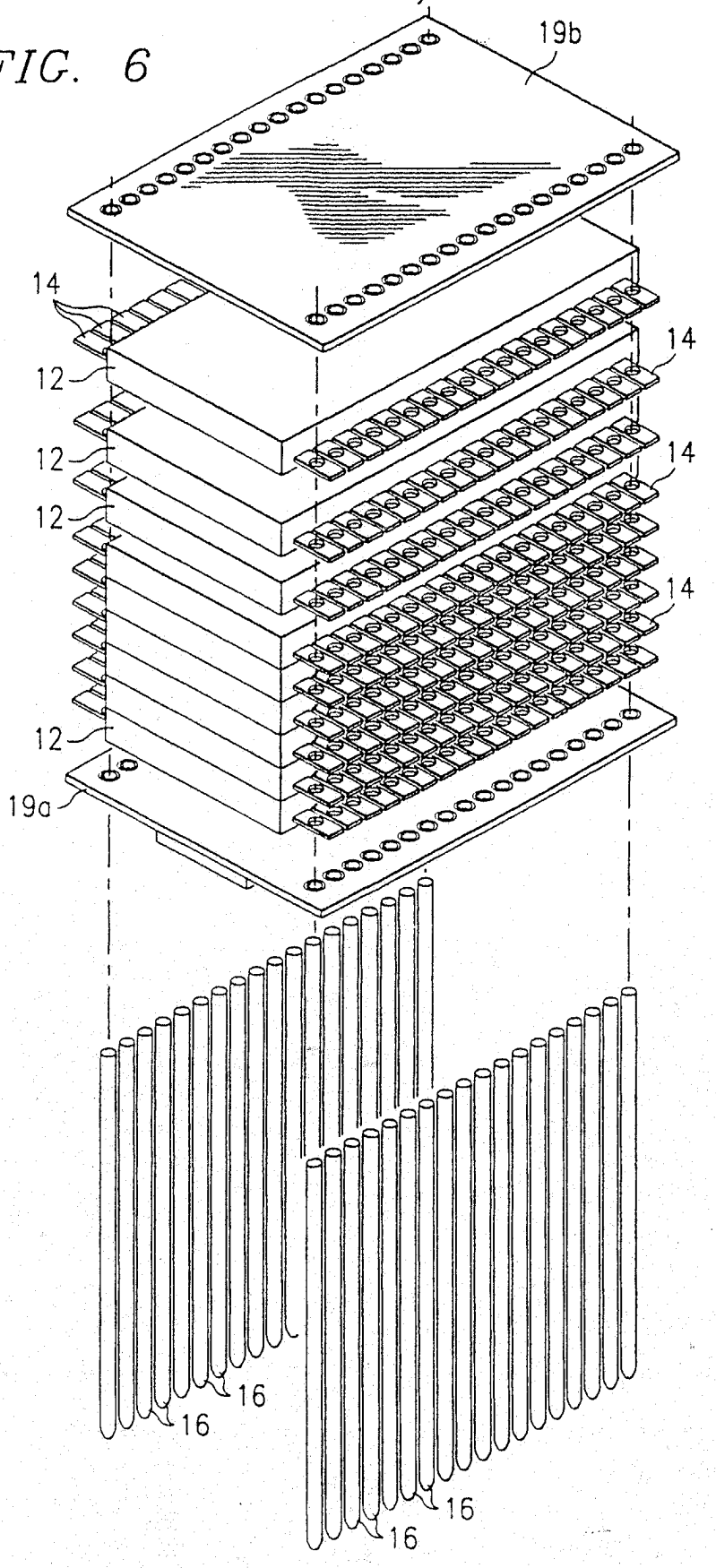


FIG. 4b

FIG. 6



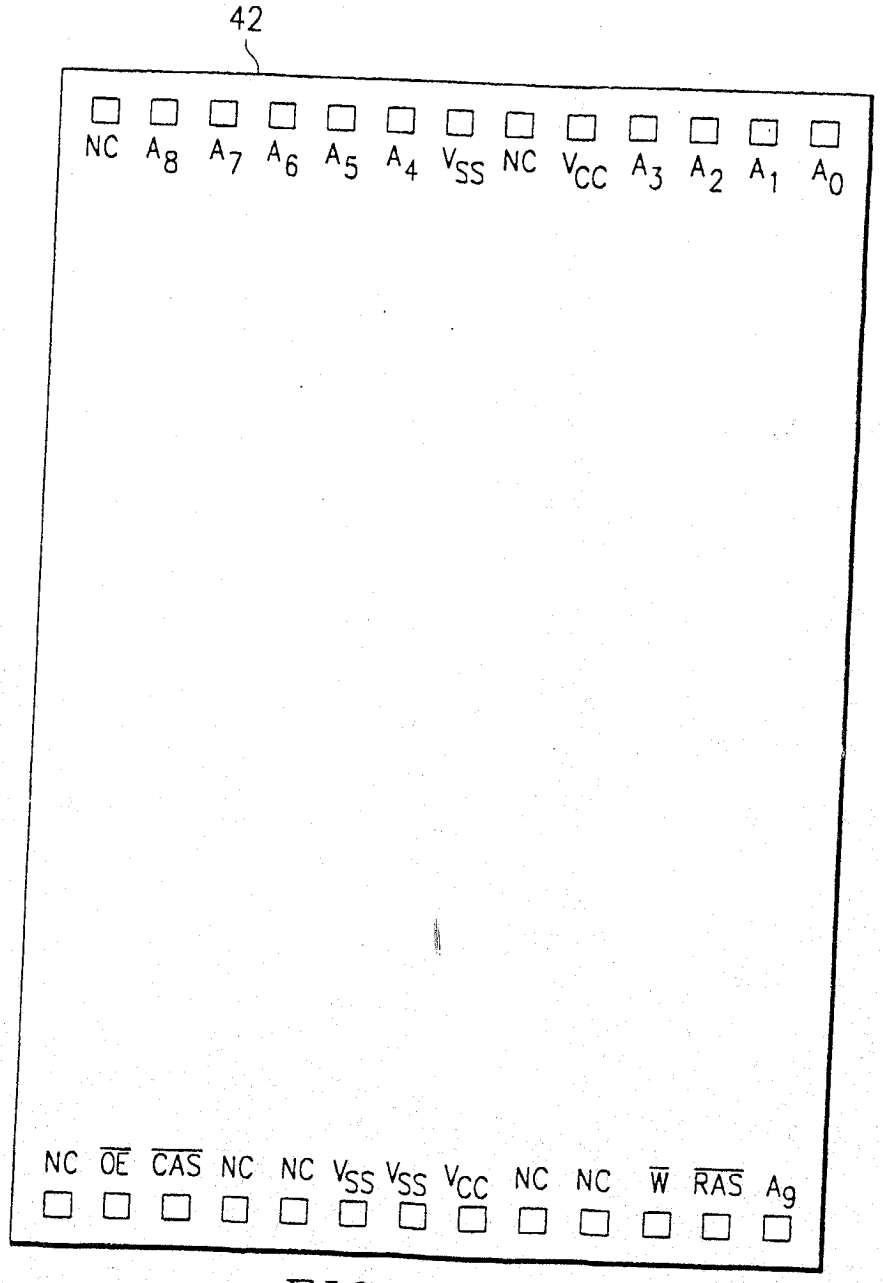
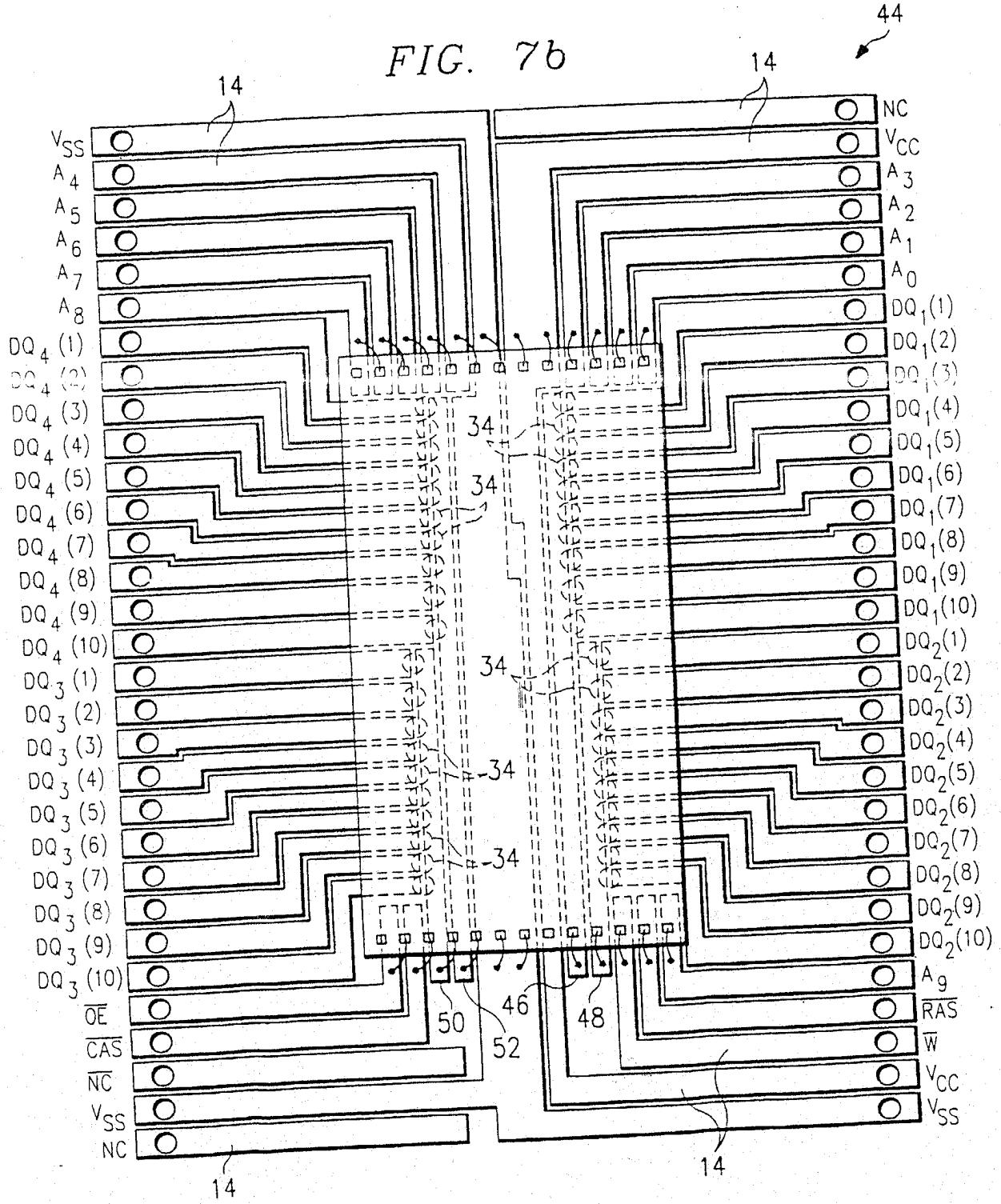

42
NC
A8
A7
A6
A5
A4
VSS
NC
VCC
A3
A2
A1
A0
NC
OE
CAS
NC
NC
VSS
VSS
VCC
NC
NC
W
RAS
A9

FIG. 7a

FIG. 7b


44
14
14
V_{SS}
A_4
A_5
A_6
A_7
A_8
DQ_4 (1)
DQ_4 (2)
DQ_4 (3)
DQ_4 (4)
DQ_4 (5)
DQ_4 (6)
DQ_4 (7)
DQ_4 (8)
DQ_4 (9)
DQ_4 (10)
DQ_3 (1)
DQ_3 (2)
DQ_3 (3)
DQ_3 (4)
DQ_3 (5)
DQ_3 (6)
DQ_3 (7)
DQ_3 (8)
DQ_3 (9)
DQ_3 (10)
$\overline{OE}$
$\overline{CAS}$
$\overline{NC}$
V_{SS}
NC
NC
V_{CC}
A_3
A_2
A_1
A_0
DQ_1(1)
DQ_1(2)
DQ_1(3)
DQ_1(4)
DQ_1(5)
DQ_1(6)
DQ_1(7)
DQ_1(8)
DQ_1(9)
DQ_1(10)
DQ_2(1)
DQ_2(2)
DQ_2(3)
DQ_2(4)
DQ_2(5)
DQ_2(6)
DQ_2(7)
DQ_2(8)
DQ_2(9)
DQ_2(10)
A_9
$\overline{RAS}$
$\overline{W}$
V_{CC}
V_{SS}
34
34
34
34
34
46
48
50
52
14
14